

REMARKS

This responds to the Office Action mailed on April 5, 2007.

Claims 1-4, 9, 13-14, 17, 20, 22-24, 27-28, 34, 36, 39, 43, 47-48, 50-51, 59 and 66 are amended, claim 63 is canceled, and claims 70 and 71 are added; as a result, claims 1-62, 64-71 are now pending in this application.

§102 Rejection of the Claims

Claims 1-18 and 20-69 were rejected under 35 U.S.C. § 102(e) for anticipation by Borland et al. (U.S. 6,724,772 B1).

Applicant submits that Borland does not describe or even suggest the invention as claimed. Independent claims 1, 22, 24, and 47 have nevertheless been amended to more clearly define the invention.

Borland describes a bus arrangement where the plurality of modules is connected in parallel. If a link between any one of the modules 210A-210H and the bus is severed, the other modules still have connectivity to the bus which can still communicate data between those module still connected to the bus. This parallel connection is clearly evident from the figures as well as the detailed description. Although Borland refers to a “circular bus” (as shown in Figures 1 and 3), the modules 210A-210H are still connected in a parallel configuration. Borland indicates that the “[b]uses 330 and 332 may be serial or parallel busses, as desired.” It will readily be understood to a person of ordinary skill in the art that a *serial bus* does not teach a serial connection between two modules but rather the manner that data is *communicated on the bus*. A serial bus sends one bit at a time as opposed to a parallel bus that send multiple bits at a time. In Borland communication of data is **not from module to module** on the busses 330 and 332 as the bus is not arranged in a ring configuration.

In stark contrast to the parallel connection of the modules 210A-210H in Borland, the invention as claimed in the present application includes a plurality of processing modules connected in a ring configuration. Hence, claim 1 included the limitation *media data is clocked*

from processing module to processing module around the data path so as to communicate from a source processing module to a target processing module” The clocking of media data from processing module to processing module around the data path so as to communicate from a source processing module to a target processing module is clearly evident from the drawings (e.g., Figures 1, 2, and 5) and the detailed description of the pending application.

Claim 22, 24, and 47 include similar limitations and it is thus submitted that Borland does also not describe each and every limitation of these claims.

In view of the above it is submitted that claims 1, 22, 24 and 47 are allowable. As dependent claims 2-21, 23, 25-46, and 48-69 are dependent upon claims 1, 22, 24, and 47 respectively, they are also allowable.

New claims 70 and 71 have been added basis for the claims can be found, *inter alia*, in Figure 5 and its associated description.

§103 Rejection of the Claims

Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Borland et al..

As discussed above, Borland does not teach or even suggest all the limitations of claim 1. Accordingly, as claim 19 which is dependent upon claim 1, it is allowable.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant’s silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference.

Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at 408-278-4041 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 5 / 30 / 2007

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 30th day of May, 2007.

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